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L4	1	716/?.ccls. and equivalence near3 check$3 and invers$3 same map$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 09:52
L5	0	716/3.ccls. and equivalence near3 check$3 and invers$3 same map$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 09:54
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L7	0	703/13-22.ccls. and equivalence near3 check$3 and invers$3 same map$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 09:53
L8	2	703/13-22.ccls. and equivalence near3 check$3 and invers$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 09:53
L9	7	716/3.ccls. and equivalence near3 check$3 and invers$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 09:54

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L10	3	L9 and @ad<"20010309"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 09:55

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IEEE STD	IEEE Standard

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1. **Is state mapping essential for equivalence checking custom memories in designs?**
Krishnamurthy, N.; Bhadra, J.; Abadir, M.S.; Abraham, J.A.;
VLSI Test Symposium, 2002. (VTS 2002). Proceedings 20th IEEE
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Digital Object Identifier 10.1109/VTS.2002.1011152
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Burch, J.R.; Singhal, V.;
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Stoffel, D.; Kunz, W.;
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10. **Efficient computation of dominators in multiple-output circuit graphs**
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11. **A fast algorithm for finding common multiple-vertex dominators in circui**
Krenz, R.; Dubrova, E.;
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12. **Improved Boolean function hashing based on multiple-vertex dominator**
Krenz, R.; Dubrova, E.;
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Fujita, M.;
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10-14 Nov. 1996 Page(s):346 - 353
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Baowen Xu; Dazhou Kang; Jianjiang Lu; Peng Wang; Yanhui Li;
Information Reuse and Integration, 2004. IRI 2004. Proceedings of the 2004 IE
Conference on
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Digital Object Identifier 10.1109/IRI.2004.1431470
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1 Using complete-1-distinguishability for FSM equivalence checking
Pranav Ashar, Aarti Gupta, Sharad Malik
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf(179.16 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper introduces the use of the Complete-1-Distinguishability (C-1-D) property for simplifying FSM verification. This property eliminates the need for a traversal of the product machine for the implementation and the specification. Instead, a much simpler check suffices. This check consists of first obtaining a 1-equivalence mapping between states of the two machines, and then checking that it is a bisimulation relation. The C-1-D property can be used directly on specifications for which it ...

Keywords: formal verification, sequential logic synthesis and verification,finite state machine equivalence, bisimulation relation, 1-distinguishability, 1-equivalence.

2 Using SAT for combinational equivalence checking
E. Goldberg, M. Prasad, R. Brayton
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: IEEE Press
Full text available: pdf(115.58 KB) Additional Information: full citation, references, citings, index terms

3 Using complete-1-distinguishability for FSM equivalence checking
Pranav Ashar, Aarti Gupta, Sharad Malik
October 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 4
Publisher: ACM Press
Full text available: pdf(286.12 KB) Additional Information: full citation, abstract, references, index terms

This article introduces the notion of a Complete-1-Distinguishability (C-1-D) property for simplifying equivalence checking of finite state machines (FSMs). When a specification machine has the C-1-D property, the traversal of the product machine can be eliminated. Instead, a much simpler check suffices. The check consists of first obtaining a 1-

equivalence mapping between the individually reachable states of the specification and the implementation machines, and then checking that it is a bisim ...

Keywords: Bisimulation relation, complete-1-distinguishability, equivalence checking, finite state machine equivalence, sequential logic synthesis

4 Query processing for XML data: Rewriting nested XML queries using nested views

Nicola Onose, Alin Deutsch, Yannis Papakonstantinou, Emiran Curtmola

June 2006 **Proceedings of the 2006 ACM SIGMOD international conference on Management of data SIGMOD '06**

Publisher: ACM Press

Full text available: pdf(394.40 KB) Additional Information: full citation, abstract, references, index terms

We present and analyze an algorithm for equivalent rewriting of XQuery queries using XQuery views, which is complete for a large class of XQueries featuring nested FLWR blocks, XML construction and join equalities by value and identity. These features pose significant challenges which lead to fundamental extension of prior work on the problems of rewriting conjunctive and tree pattern queries. Our solution exploits the Nested XML Tableaux (NEXT) notation which enables a logical foundation for sp ...

Keywords: XML nested query, reformulation, rewriting, views

5 Layout-driven Timing Optimization by Generalized De Morgan Transform

Supratik Chakraborty, Rajeev Murgai

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Publisher: IEEE Computer Society

Full text available: pdf(157.58 KB) Publisher Site Additional Information: full citation, abstract

We propose a timing-oriented logic optimization technique called Generalized De Morgan (GDM) transform, that integrates gate resizing, net buffering and De Morgan transformation. The contribution of our work lies in the integration of the three techniques, allowing them to interact at a much finer level of granularity than would be otherwise possible. This produces better results than those obtainable by individual techniques like net buffering or gate resizing applied to the circuit in various ...

Keywords: Timing optimization, timing closure, layout-driven optimization, in-place circuit optimization, DeMorgan transformation, deep sub-micron design

6 On equivalence and canonical forms in the LF type theory

Robert Harper, Frank Pfenning

January 2005 **ACM Transactions on Computational Logic (TOCL)**, Volume 6 Issue 1

Publisher: ACM Press

Full text available: pdf(243.65 KB) Additional Information: full citation, abstract, references, citings, index terms

Decidability of definitional equality and conversion of terms into canonical form play a central role in the meta-theory of a type-theoretic logical framework. Most studies of definitional equality are based on a confluent, strongly normalizing notion of reduction. Coquand has considered a different approach, directly proving the correctness of a practical equivalance algorithm based on the shape of terms. Neither approach appears to scale well to richer languages with, for example, unit types o ...

Keywords: Logical frameworks, type theory

7 Proofs by structural induction using partial evaluation

Julia L. Lawall
August 1993 **Proceedings of the 1993 ACM SIGPLAN symposium on Partial evaluation and semantics-based program manipulation**
Publisher: ACM Press

Full text available: pdf(1.00 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we show how partial evaluation can be used in developing proofs about program transformations. Partial evaluation is particularly appropriate for this task because it distinguishes between static and dynamic data. As a realistic example of this technique we prove a theorem arising in our earlier study of the CPS transformation. Our approach requires a partial evaluator that supports the following features: resugaring, partially-static structures, higher-order functions, polyva ...

8 An efficient equivalence checker for combinational circuits

Yusuke Matsunaga
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(189.35 KB) Additional Information: full citation, references, citings, index terms

9 Rules and strategies for transforming functional and logic programs

Alberto Pettorossi, Maurizio Proietti
June 1996 **ACM Computing Surveys (CSUR)**, Volume 28 Issue 2
Publisher: ACM Press

Full text available: pdf(763.99 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We present an overview of the program transformation methodology, focusing our attention on the so-called "rules + strategies" approach in the case of functional and logic programs. The paper is intended to offer an introduction to the subject. The various techniques we present are illustrated via simple examples.

Keywords: program derivation, program improvement, transformation rules, transformation strategies

10 Consistency checking for MOS/VLSI circuits

Ning-Sang Chang, Ravi M. Apte
June 1983 **Proceedings of the 20th conference on Design automation**
Publisher: IEEE Press
Full text available: pdf(205.40 KB) Additional Information: full citation, abstract, references, index terms

A general algorithm is presented for consistency checking between schematics. A transistor level schematic is partitioned into functional blocks by tracing direct current paths. The first level consistency check is performed on the directed graphs constructed from these functional blocks. A recursive, graph matching algorithm is introduced to find signal correspondences in the functional blocks. The second level check is performed within the functional blocks for either identical component ...

11 Session 10C: flexibility in logic synthesis: Generalized symmetries in boolean

functions
Victor N. Kravets, Karem A. Sakallah
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press
Full text available: pdf(134.37 KB) Additional Information: full citation, abstract, references, citings

In this paper we take a fresh look at the notion of symmetries in Boolean functions. Our studies are motivated by the fact that the classical characterization of symmetries based on invariance under variable swaps is a special case of a more general invariance based on unrestricted variable permutations. We propose a generalization of classical symmetry that allows for the simultaneous swap of ordered and unordered groups of variables, and show that it captures more of a function's invariant per ...

12 Array Permutation by Index-Digit Permutation
Donald Fraser
April 1976 **Journal of the ACM (JACM)**, Volume 23 Issue 2
Publisher: ACM Press
Full text available: pdf(806.68 KB) Additional Information: full citation, abstract, references, citings, index terms

An array may be reordered according to a common permutation of the digits of each of its element indices. The digit-reversed reordering which results from common fast Fourier transform (FFT) algorithms is an example. By examination of this class of permutation in detail, very efficient algorithms for transforming very long arrays are developed.

13 A semantics for web services authentication
Karthikeyan Bhargavan, Cédric Fournet, Andrew D. Gordon
January 2004 **ACM SIGPLAN Notices , Proceedings of the 31st ACM SIGPLAN-SIGACT symposium on Principles of programming languages POPL '04**, Volume 39 Issue 1
Publisher: ACM Press
Full text available: pdf(234.06 KB) Additional Information: full citation, abstract, references, citings, index terms

We consider the problem of specifying and verifying cryptographic security protocols for XML web services. The security specification WS-Security describes a range of XML security tokens, such as username tokens, public-key certificates, and digital signature blocks, amounting to a flexible vocabulary for expressing protocols. To describe the syntax of these tokens, we extend the usual XML data model with symbolic representations of cryptographic values. We use predicates on this data model to d ...

Keywords: XML security, applied pi calculus, web services

14 Atomicity and isolation for transactional processes
Heiko Schuldt, Gustavo Alonso, Catriel Beeri, Hans-Jörg Schek
March 2002 **ACM Transactions on Database Systems (TODS)**, Volume 27 Issue 1
Publisher: ACM Press
Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, citings, index terms

Processes are increasingly being used to make complex application logic explicit. Programming using processes has significant advantages but it poses a difficult problem from the system point of view in that the interactions between processes cannot be controlled using conventional techniques. In terms of recovery, the steps of a process are different from operations within a transaction. Each one has its own termination semantics and there are dependencies among the different steps. Regarding c ...

Keywords: Advanced transaction models, business process management, electronic commerce, execution guarantees, locking, rocesses, semantically rich transactions, transactional workflows, unified theory of concurrency control and recovery

15 Equivalence checking using cuts and heaps

Andreas Kuehlmann, Florian Krohm
June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**
Publisher: ACM Press
Full text available: pdf(229.44 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents a verification technique which isspecifically targeted to formally comparing large combinational circuits with some structural similarities. The approach combines the application of BDDs withcircuit graph hashing, automatic insertion of multiple cut frontiers, and a controlled elimination of false negative verification results caused by the cuts. Twoideas fundamentally distinguish the presented technique from previous approaches. First, originating from the cut frontiers, mul ...

16 Using 2-domain partitioned OBDD data structure in an enhanced symbolic simulator

Tao Feng, Li-C Wang, Kwang-Ting (Tim) Cheng, Chih-Chang (Andy) Lin
October 2005 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 10 Issue 4
Publisher: ACM Press
Full text available: pdf(419.60 KB) Additional Information: full citation, abstract, references, index terms

In this article, we propose a symbolic simulation method where Boolean functions can be efficiently manipulated through a 2-domain partitioned OBDD data structure. The functional partition is applied by automatically exploring the key decision points implicitly built inside a circuit. The partition can help to significantly reduce the OBDD sizes, solving problems that could not be solved with monolithic OBDD data structure. We demonstrate the performance of the approach through the symbolic simu ...

Keywords: Formal verification, equivalence checking, symbolic simulation

17 Free Kronecker decision diagrams and their application to Atmel 6000 series FPGA mapping

Marek A. Perkowski, Philip Ho
September 1994 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(729.77 KB) Additional Information: full citation, references, index terms

18 Composite model-checking: verification with type-specific symbolic representations

Tevfik Bultan, Richard Gerber, Christopher League
January 2000 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 9 Issue 1
Publisher: ACM Press
Full text available: pdf(400.17 KB) Additional Information: full citation, abstract, references, citings, index terms

There has been a surge of progress in automated verification methods based on state exploration. In areas like hardware design, these technologies are rapidly augmenting key phases of testing and validation. To date, one of the most successful of these methods

has been symbolic model-checking, in which large finite-state machines are encoded into compact data structures such as Binary Decision Diagrams (BDDs), and are then checked for safety and liveness properties. However, these technique ...

Keywords: Presburger arithmetic, binary decision diagrams, symbolic model-checking

19 Restricted data types, specification and enforcement of invariant properties of variables

Normand Buckle

March 1977 **ACM SIGPLAN Notices , ACM SIGSOFT Software Engineering Notes , ACM SIGOPS Operating Systems Review , Proceedings of an ACM conference on Language design for reliable software**, Volume 12 , 2 , 11 Issue 3 , 2 , 2

Publisher: ACM Press

Full text available: pdf(837.35 KB) Additional Information: full citation, abstract, references, citings, index terms

When defining a data type, it is often useful to specify restrictions on the permitted values of that type. Pascal's subrange type declaration, a special case of this kind of constraint definition, has already proved itself to be quite useful. Restricted data types allow more complex constraints to be defined and checked; for example, a variable could be declared of type "odd integer" or the day field of a "date" type variable could be checked for consiste ...

Keywords: Data type, Invariant property, Programming language, Readability, Reliability, Restricted type, Runtime verification, Type checking

20 Advanced verification techniques based on learning

Jawahar Jain, Rajarshi Mukherjee, Masahiro Fujita

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Publisher: ACM Press

Full text available: pdf(212.78 KB) Additional Information: full citation, references, citings, index terms

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